REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated May 10, 2005. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due consideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-5 and 21-22 are under consideration in this application. Claims 1-5 and 21-22 are being cancelled without prejudice or disclaimer. New claims 23-28 are being added to recite the embodiments described in the specification and depicted in Figs. 1-8, the elected species. Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

Prior Art Rejections

Claims 1-5 and 21 were rejected under 35 U.S.C. §102(b) as being anticipated by US Patent No. 5,059,899 of Farnworth et al. (hereinafter "Farnworth"). The references Sakumoto et al. (5,239,191) was cited as pertinent to the application. This rejection has been carefully considered, but is most respectfully traversed.

The semiconductor integrated circuit device of the invention (for example, the embodiment depicted in Fig. 1), as now recited in claim 22, comprises: a semiconductor chip 1 embedded in the semiconductor integrated circuit device. The semiconductor chip 1 comprising: a first bonding pad arranged on a first side (e.g., the upper side) of the semiconductor chip 1; a second bonding pad 311 arranged on a second side (e.g., the left side) of the semiconductor chip; a first input and output buffer 4 and a second input and output buffer which are coupled to the first and second bonding pads respectively; a first inspection pad 211; a first connecting wire 411 which is laid outside an area where the first and second input and output buffers are arranged and which connects the second bonding pad 311 to the first inspection pad 211. The first inspection pad 211 is arranged on the first side (e.g., the upper side) of the semiconductor chip.

As the first inspection pad 211 (wired with the second bonding pad 311) is arranged on the first/same side of the chip as the first bonding pad, the first and second bonding pads can be probed simultaneously with probes lined in one direction on the first side, despite the

first and second bonding pads being arranged on different sides of the chip. Accordingly, the invention probes the chips quickly without using probe cards of special shapes (P. 5, lines 4-14) and reduces the cost in manufacturing the chips.

Applicants respectfully contend Farnworth fails to teach or suggest "a bonding pad and an inspection pad arranged on one side of a semiconductor chip, while the inspection pad being wired with another bonding pad arranged on another side of the semiconductor chip" as the invention.

In contrast, Farnsworth's interface test pad 20/36 is arranged in the scribe area (col. 2, lines 46-47; col. 3, lines 51-52) outside of the semiconductor chip 12/30, rather than comprised inside of the semiconductor chip as the first inspection pad 211 of the invention. In addition, Farnsworth's interface test pad 20/36 is connected to bonding pads 34 in different semiconductor chips 12/30 (Figs. 2-3), rather than bonding pads in two different sides of the same semiconductor chip 1 of the invention. Farnsworth further does not show a semiconductor chip having a bonding pad and an inspection pad arranged on the same side of the semiconductor chip, nor show a second bonding pad arranged on another side of the same chip wired/connected to the inspection pad. Thus, Farnsworth cannot simultaneously probe bonding pads arranged on different sides of the same chip with probes aligned in one direction on the first side so as to increase the probing speed and reduce the probing cost as does the invention.

Applicants contend that Farnworth fails to teach or disclose each and every feature of the present invention as disclosed in independent claim 22. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the

prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive, Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

September 22, 2005

SPF/JCM/JT